In the Specification:

Please amend the specification as follows:

Page 8, lines 7-9: For example, the same operation on different data is treated as two programs, different operations on the same data represent two programs, or different operations on different ~~operations~~ data are two programs.)

Page 15, lines 8-10: Instructions from instruction memory 203 are provided to instruction decode 204 and ~~thence~~ then to an appropriate one of registers 205A through 205N.

Page 15, line 22 - Page 16, line 1: The program counters and registers are assigned to each program and one instruction for each program is routed into the pipeline ~~each~~ clock.

Page 16, lines 19-20: A solution ~~would be~~ would be a register dependency checking, renaming, etc.

Page 16, lines 22- page 17, line 1: Since load ~~dest~~ destination could be only temp, it is possible to keep a list of load targets (for each thread), and compare each of 3 sources to each pending load, and stall on collision or the Nth pending load.